Docket No.: SCEI 3.0-170
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Keisuke Inoue

Application No.: 10/812,177 Group Art Unit: 2128

Filed: March 29, 2004 Examiner: S. A. Alhija

For: METHODS AND APPARATUS FOR ACHIEVING THERMAL MANAGEMENT USING PROCESSING TASK SCHEDULING

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

Appellant hereby file this brief on Appeal to appeal from the final rejection of claims 1-11, 13-24, 26-31, 33-60 and 63-89 mailed February 4, 2008. A petition for a two (2) month extension of time is submitted herewith.

REAL PARTY(IES) IN INTEREST

This application is assigned to Sony Computer Entertainment Inc. by the Assignment recorded July 9, 2004, at Reel 014835, Frame 0586.

RELATED APPEALS AND INTERFERENCES

No prior or pending appeals, interferences, or judicial proceedings are known to be related to, directly affect, or be directly affected by, or have a bearing on, the Board's decision in the present appeal.

STATUS OF CLAIMS

Claims 1-89 were originally filed in the instant application on March 29, 2004. Claims 12, 25, 32, 61 and 62 were cancelled during prosecution. Claims 1-11, 13-24, 26-31, 33-60 and 63-89 stand rejected. Appellant appeals from the rejections in the Office Action dated February 4, 2008. All of the pending claims, *i.e.* claims 1-11, 13-24, 26-31, 33-60 and 63-89, are being appealed.

STATUS OF AMENDMENTS

A first Office Action issued on May 3, 2007 rejecting claims 1-89. An amendment dated June 21, 2007 was filed in response to the May 3, 2007 Office Action in which claims 1, 24, 26-29, 33 and 53 were amended and claims 12, 25, 32, 61 and 62 were cancelled.

A second Office Action issued on September 11, 2007, finally rejecting 1-11, 13-24, 26-31, 33-60 and 63-89. A Notice of Appeal was filed on October 16, 2007 appealing from the final rejection.

On October 31, 2007, a Request for Continued Examination was filed, obviating the October 16, 2007 Notice of Appeal. A reply to the second Office Action was filed concurrently with the Request for Continued Examination. No amendments to the claims were made in this reply.

A third Office Action issued on February 4, 2008, again rejecting claims 1-11, 13-24, 26-31, 33-60 and 63-89. A new Notice of Appeal was then filed on February 26, 2008.

SUMMARY OF CLAIMED SUBJECT MATTER

The instant application relates generally to performing thermal management for a computer apparatus. Methods and apparatuses are provided for scheduling or otherwise managing operations/tasks based on thermal and/or cooling attributes as well as on the thermal threshold of a component.

With regard to the claims on appeal (*i.e.*, claims 1-11, 13-24, 26-31, 33-60 and 63-89), claims 1, 13, 24, 35, 44, 50, 53, 64, 65, 66 and 76 are independent. The rejections of dependent claims 2, 6, 9, 31 and 63 are argued separately below.

The subject matter of claim 1 is directed to a method of scheduling operations to be performed by a component (102 in FIG. 1; p.17, l.26 to p.18, l.20) having a thermal threshold (T_{max} in FIGS. 2A-B; p.21, l.17 to p.22, l.2) comprising: providing a plurality of operations to be performed by the component (A, B and C in FIG. 2A; p.18, ll.21-26); associating the operations with a thermal attribute, the thermal attribute representing a value related to a heat amount expected to be generated or incurred by the component during performance of the operations (FIGS. 10A-B; p.18, l.27 to p.19, l.26); determining a cooling attribute (p.24, l.12 to p.26, l.2); scheduling the operations in an order of performance based on the thermal attribute and the cooling attribute so that the thermal threshold is not exceeded (FIGS. 2A and 11; p.20, l.23 to p.21, l.16; p.22, ll.3-17); and generating the order of performance for use in execution of the operations (FIG. 2B; p.22, l.22 to p.23, l.22).

The subject matter of claim 2 is directed to measuring the thermal attribute with a temperature sensing means (p.19, ll.1-5; p.28, l.26 to p.29, l.16). The limitation "temperature

sensing means" is in means-plus-function format. The structures in the specification in support of this means-plus-function recitation include a thermometer or other temperature sensing device such as a thermal sensor.

The subject matter of claim 6 is directed to a component executing the operations in the order of performance (steps 606 and 610 of FIG. 6; p.30, l.8 to p.31, l.3).

The subject matter of claim 9 is directed to selecting at least some of the processing devices to execute the operations (FIG. 9A; p.33, l.3 to p.34, l.9); monitoring the selected processing devices (FIG. 11; p.25, l.5 to p.26, l.2; p.28, l.26 to p.29, l.16); and routing the operations among the selected processing devices so that the individual thermal thresholds are not exceeded (FIGS. 9B-C; p.33, l.10 to p.34, l.9).

The subject matter of claim 13 is directed to a thermal scheduling method, which includes obtaining program code (FIG. 11; p.20, l.23 to p.21, l.16) including a series of operations (A, B and C in FIGS. 2A-B; Tasks H_1-H_N and Tasks C_1-C_N in FIG. 5; p.21, l.17 to p.22, l.17; p.27, l.5 to p.28, l.9); determining thermal attributes (table at lines 13-19 preceding paragraph 0073 at p.20) associated with one or more of the operations (FIGS. 5 and 7; p.18, ll.27-34; p.19, l.1 to p.20, l.18); determining a thermal threshold (T_{max} in FIGS. 2A, 2B and 6; p.21, l.17 to p.22, l.2; p.30, l.8 to p.31, l.3) for a component (102, 104 and 106 in FIG. 1; p.17, l.26 to p.18, l.20); and scheduling the operations for execution by the component in accordance with the thermal attributes so that the thermal threshold is not exceeded (A, B and C in FIG. 2B; steps 602-610 in FIG. 6; steps 802-810 in FIG. 8; Tasks 1-3 in FIGS. 9A-C; FIG. 11; p.20, l.23 to p.21, l.16; p.22, ll.3-21; p.30, l.8 to p.31, l.3; p.31, l.22 to p.32, l.28).

The subject matter of claim 24 is directed to a processing system (300 and 350-364 in FIGS. 3A-B; 400 in FIG. 4; 540 in FIG. 7; PE1-PE4 in FIGS. 9A-C; and SPU 400 in FIGS. 10A-B; p.14, l.14 to p.17, l.25) comprising a computing device including a component (102, 104 and 106 in FIG. 1; 300, 304 and 308a-308d in FIG. 3A; 350 in FIG. 3B; p.14, l.59 to p.16, l.16; p.17, l.26 to p.18, l.20); a plurality of operations to be performed by the component (A, B and C in FIGS. 2A-B; Tasks H_1-H_N and Tasks C_1-C_N in FIG. 5; p.21, l.17 to p.22, l.17; p.27, l.5 to p.28, l.9), at least some of the operations including a priority (Tasks H_{1H}-H_{NH} and Tasks C_{1H}-C_{NH} in block 544, Tasks H_{1M}-H_{NM} and Tasks C_{1M}-C_{NM} in block 546, and Tasks H_{1L}-H_{NL} and Tasks C_{1L}-C_{NL} in block 548 in FIG. 7; p.31, ll.4-21); at least one thermal attribute associated with the component and a selected one of the operations, the thermal attribute being indicative of a change in temperature of the component after performance of the selected operation (table at lines 13-19 preceding paragraph 0073 at p.20; FIGS. 5 and 7; p.18, ll.27-34; p.19, l.1 to p.20, l.18); a plurality of priority queues, each priority queue including a first queue and a second queue, the first queue for storing a first set of the operations and the second queue for storing a second set of the operations (504 and 506 in FIG. 5; 544, 546 and 548 in FIG. 7; p.26, l.3 to p.27, l.4; p.31, ll.4-21); and a scheduler operable to assign at least one of the operations to the component depending on the thermal attribute (502 in FIG. 5; 542 in FIG. 7; p.27, l.5 to p.30, l.7; p.31, ll.4-12).

The subject matter of claim 31, which depends from claims 24 and 30, is directed to having a task thermal attribute based on at least one of an operating frequency of the component, a thermal attribute of the component, and a cooling attribute (p.24, l.12 to p.25, l.2; p.27, l.28 to p.28, l.1).

The subject matter of claim 35 is directed to a processing system (500 in FIG. 5; 540 in FIG. 7), comprising a first operation having a first thermal attribute exceeding an operating threshold (Tasks H_1-H_N in 504 of FIG. 5; Tasks H_{1H}-H_{NH} in block 544, Tasks H_{1M}-H_{NM} in block 546, and Tasks H_{1L}-H_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); a second operation having a second thermal attribute not exceeding the operating threshold (Tasks C_1-C_N in 506 of FIG. 5; Tasks C_{1H}-C_{NH} in block 544, Tasks C_{1M}-C_{NM} in block 546, and Tasks C_{1L}-C_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); a scheduler for managing a plurality of operations comprising the first and second operations based on the thermal attributes (502 in FIG. 5; 542 in FIG. 7; p.27, l.5 to p.30, l.7; p.31, ll.4-12); and a plurality of processors for executing the plurality of operations, each of the plurality of processors having a thermal threshold (PE_1, PE_N, PU_1, PU_N, SPU_1 and SPU_N in FIGS. 5 and 7; p.28, l.26 to p.29, l.16; p.31, l.24 to p.32, l.28).

The subject matter of claim 44 is directed to a method of performing operations in a computing environment (600 in FIG. 6; 800 in FIG. 8; p.30, l.8 to p.31, l.3; p.31, l.22 to p.32, l.28), comprising: storing a first operation based upon a thermal attribute of the first operation (504 ("Hot Queue") of FIG. 5; 544, 546 and 548 ("Hot Queue") of FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); storing a second operation based upon a thermal attribute of the second operation (506 ("Cool Queue") of FIG. 5; 544, 546 and 548 ("Cool Queue") of FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); and retrieving at least one of the first and the second operations (A, B and C of FIG. 2B; Tasks 1-3 of FIGS. 9A-C; p.22, ll.8-21; p.33, ll.3-9) depending upon a thermal threshold of a processor (T_{max} of FIG. 2B; PE 1 - PE 4 of FIGS. 9A-C; p.22, ll.8-21; p.33, l.10 to p.34, l.9).

The subject matter of claim 50 is directed to method of performing operations in a computing environment (600 in FIG. 6; 800 in FIG. 8; p.30, l.8 to p.31, l.3; p.31, l.22 to p.32, l.28), comprising: determining if a temperature of a processor exceeds a thermal threshold (A, B and C in FIG. 2B; steps 602-610 in FIG. 6; steps 802-810 in FIG. 8; Tasks 1-3 in FIGS. 9A-C; FIG. 11; p.20, l.23 to p.21, l.16; p.22, ll.3-21; p.30, l.8 to p.31, l.3; p.31, l.22 to p.32, l.28); and (i) if the thermal threshold is not exceeded: determining if a first operation is available, the first operation being likely to maintain or increase the temperature of the processor upon execution (604 in FIG. 6; 802 in FIG. 8; p.30, ll.8-17; p.31, ll.27-34); and if the first operation is available, executing the first operation (606 in FIG. 6; 806 in FIG. 8; p.30, ll.17-19; p.31, l.33 to p.32, l.2); (ii) if the thermal threshold is exceeded: determining if a second operation is available, the second operation being likely to decrease the temperature of the processor upon execution (608 in FIG. 6; 808 in FIG. 8; p.30, ll.19-23; p.32, ll.3-7); and if the second operation is available, executing the second operation (610 in FIG. 6; 810 in FIG. 8; p.30, ll.23-25; p.32, ll.7-9).

The subject matter of claim 53 is directed to processing apparatus for processing operations associated with thermal attributes (300 and 350-364 in FIGS. 3A-B; 400 in FIG. 4; 500 in FIG. 5; 540 in FIG. 7; PE1-PE4 in FIGS. 9A-C; and SPU 400 in FIGS. 10A-B; p.14, l.14 to p.17, l.25; p.26, l.3 to p.30, l.7), comprising: a memory for storing a first operation and a second operation (330 in FIG. 3A; 358 in FIG. 3B; 402 in FIGS. 4, 10A and 10B; p.14, l.33 to p.15, l.8; p.16, ll.1-2; p.16, l.17 to p.17, l.6), the first operation having a thermal attribute exceeding an operating threshold (Tasks H_1-H_N in 504 of FIG. 5; Tasks H_{1H}-H_{NH} in block 544, Tasks H_{1M}-H_{NM} in block 546, and

Tasks H_{1L}-H_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21), and the second operation having a thermal attribute not exceeding the operating threshold (Tasks C_1-C_N in 506 of FIG. 5; Tasks C_{1H}-C_{NH} in block 544, Tasks C_{1M}-C_{NM} in block 546, and Tasks C_{1L}-C_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); and a plurality of processing devices for executing the first and second operations, at least a selected one of the processing devices comprising a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the memory (300, 304 and 308a-308d in FIG. 3A; 350 in FIG. 3B; p.14, l.59 to p.16, l.16; p.17, l.26 to p.18, l.20); wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device is operable to obtain the first operation from the memory for processing and to process the first operation (604 and 606 in FIG. 6; 802 and 806 in FIG. 8; p.30, ll.8-19; p.31, l.27 to p.32, l.2), and if the thermal threshold of the selected processing device is exceeded, the selected processing device is operable to obtain the second operation from the memory for processing and to process the second operation (608 and 610 in FIG. 6; 808 and 810 in FIG. 8; p.30, ll.19-25; p.32, ll.3-9), and wherein the memory comprises a local store in the sub-processing unit, and the local store includes a first queue for managing the first operation and a second queue for managing the second operation (402 in FIGS. 4, 10A and 10B; p.16, l.17 to p.17, l.6; p.26, ll.17-29).

The subject matter of claim 63, which depends from claim 53, is directed to the first and second operations being maintained in the memory in a timesharing arrangement (p.26, l.34 to p.27, l.4).

The subject matter of claim 64 is directed to a processing apparatus for processing operations associated with

thermal attributes (300 and 350-364 in FIGS. 3A-B; 400 in FIG. 4; 500 in FIG. 5; 540 in FIG. 7; PE1-PE4 in FIGS. 9A-C; and SPU 400 in FIGS. 10A-B; p.14, l.14 to p.17, l.25; p.26, l.3 to p.30, l.7), comprising: first and second memories for storing first and second operations (330 in FIG. 3A; 358 in FIG. 3B; 402 in FIGS. 4, 10A and 10B; p.14, l.33 to p.15, l.8; p.16, ll.1-2; p.16, l.17 to p.17, l.6), the first operation having a thermal attribute exceeding an operating threshold (Tasks H_1-H_N in 504 of FIG. 5; Tasks H_{1H}-H_{NH} in block 544, Tasks H_{1M}-H_{NM} in block 546, and Tasks H_{1L}-H_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21), and the second operation having a thermal attribute not exceeding the operating threshold (Tasks C_1-C_N in 506 of FIG. 5; Tasks C_{1H}-C_{NH} in block 544, Tasks C_{1M}-C_{NM} in block 546, and Tasks C_{1L}-C_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); a plurality of processing devices for executing the first and second operations, at least a selected one of the processing devices comprising a processing element, a processing unit or a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the first and second memories (300, 304 and 308a-308d in FIG. 3A; 350 in FIG. 3B; p.14, l.59 to p.16, l.16; p.17, l.26 to p.18, l.20); wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device obtains the first operation from either the first memory or the second memory for processing (604 and 606 in FIG. 6; 802 and 806 in FIG. 8; p.30, ll.8-19; p.31, l.27 to p.32, l.2), and if the thermal threshold of the selected processing device is exceeded, the selected processing device obtains the second operation from either the first memory or the second memory for processing (608 and 610 in FIG. 6; 808 and 810 in FIG. 8; p.30, ll.19-25; p.32, ll.3-9).

The subject matter of claim 65 is directed to a processing apparatus for processing operations associated with thermal attributes (300 and 350-364 in FIGS. 3A-B; 400 in FIG. 4; 500 in FIG. 5; 540 in FIG. 7; PE1-PE4 in FIGS. 9A-C; and SPU 400 in FIGS. 10A-B; p.14, l.14 to p.17, l.25; p.26, l.3 to p.30, l.7), comprising: first and second memories for storing first and second sets of the operations (330 in FIG. 3A; 358 in FIG. 3B; 402 in FIGS. 4, 10A and 10B; p.14, l.33 to p.15, l.8; p.16, ll.1-2; p.16, l.17 to p.17, l.6), the first memory including a first queue for managing the first set of operations (504 in FIG. 5; 544, 546 and 548 in FIG. 7; p.26, l.5 to p.28, l.9; p.31, ll.7-21), the second memory including a second queue for managing the second set of operations (506 in FIG. 5; 544, 546 and 548 in FIG. 7; p.26, l.5 to p.28, l.9; p.31, ll.7-21), the first set of operations having thermal attributes exceeding an operating threshold (Tasks H_1-H_N in 504 of FIG. 5; Tasks H_{1H}-H_{NH} in block 544, Tasks H_{1M}-H_{NM} in block 546, and Tasks H_{1L}-H_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21), and the second set of operations having thermal attributes not exceeding the operating threshold (Tasks C_1-C_N in 506 of FIG. 5; Tasks C_{1H}-C_{NH} in block 544, Tasks C_{1M}-C_{NM} in block 546, and Tasks C_{1L}-C_{NL} in block 548 in FIG. 7; p.27, l.5 to p.28, l.9; p.31, ll.4-21); a plurality of processing devices for executing the first and second sets of operations, at least a selected one of the processing devices comprising a processing element, a processing unit or a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the first and second memories (300, 304 and 308a-308d in FIG. 3A; 350 in FIG. 3B; p.14, l.59 to p.16, l.16; p.17, l.26 to p.18, l.20); wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device obtains at least one of the first set of operations for processing (604 and 606 in FIG. 6; 802 and 806 in FIG. 8; p.30,

ll.8-19; p.31, l.27 to p.32, l.2), and if the thermal threshold of the selected processing device is exceeded, the selected processing device obtains at least one of the second set of operations for processing (608 and 610 in FIG. 6; 808 and 810 in FIG. 8; p.30, ll.19-25; p.32, ll.3-9).

The subject matter of claim 66 is directed to a method of processing tasks (600 in FIG. 6; 800 in FIG. 8; p.30, l.8 to p.31, l.3; p.31, l.22 to p.32, l.28) comprising: selecting one of a plurality of tasks for execution by a component based on an attribute (602, 604 and 608 of FIG. 6; 802, 804 and 808 of FIG. 8; p.30, l.8 to p.31, l.3; p.31, l.27 to p.32, l.7) wherein the attribute for each task is related to the temperature of the component after execution of the associated task (Attributes in FIGS. 10A-B; p.18, l.27 to p.20, l.29; p.23, l.23 to p.24, l.5); and executing the selected task (606 and 610 in FIG. 6; 806 and 810 in FIG. 8; p.30, ll.17-19; p.30, ll.23-25; p.31, l.33 to p.32, l.2; p.32, ll.7-9).

The subject matter of claim 76 is directed to a system for processing tasks (300 and 350-364 in FIGS. 3A-B; 400 in FIG. 4; 500 in FIG. 5; 540 in FIG. 7; PE1-PE4 in FIGS. 9A-C; and SPU 400 in FIGS. 10A-B; p.14, l.14 to p.17, l.25; p.26, l.3 to p.30, l.7) comprising: memory for storing tasks to be processed (330 in FIG. 3A; 358 in FIG. 3B; 402 in FIGS. 4, 10A and 10B; p.14, l.33 to p.15, l.8; p.16, ll.1-2; p.16, l.17 to p.17, l.6); a component that processes the tasks stored in the memory (300, 304 and 308a-308d in FIG. 3A; 350 in FIG. 3B; p.14, l.59 to p.16, l.16; p.17, l.26 to p.18, l.20); wherein the tasks are associated with attributes, the attribute for each task is related to the temperature of the component after processing the associated task (Attributes in FIGS. 10A-B; p.18, l.27 to p.20, l.29; p.23, l.23 to p.24, l.5), and one of the tasks is chosen for processing by the component based on the attribute (602, 604

and 608 of FIG. 6; 802, 804 and 808 of FIG. 8; p.30, l.8 to p.31, l.3; p.31, l.27 to p.32, l.7).

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Whether the § 112, second paragraph multiplicity rejection of claims 1-11, 13-24, 26-31, 33-60 and 63-89 is valid.

II. Whether the § 101 rejection of claims 1-11, 24, 26-31, 33-34, 53-60 and 63 is valid.

III. Whether claims 1-11, 24, 26-31, 33-34, 53-60 and 63 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent Publication No. 2002/0065049 ("*Chauvel*").

ARGUMENT

I. The § 112, Second Paragraph Multiplicity Rejection of Claims 1-11, 13-24, 26-31, 33-60 and 63-89

The February 4, 2008 Office Action rejected all pending claims "by virtue of undue multiplicity." (Office Action, p.6, numbered section 4.) In support of the rejection, the Office Action then quoted a portion of section 2173.05(n) of the Manual of Patent Examining Procedure ("MPEP"). Unfortunately, the rejection failed to quote the next sentence in this section of the MPEP, which states "[u]ndue multiplicity rejections based on 35 U.S.C. § 112, second paragraph, should be applied judiciously and should be rare." Appellant submits that the multiplicity rejection was not judiciously applied as it is without basis and should be reversed.

The Office Action stated:

> The now 84 claims and 11 independent claims contain limitations from multiple embodiments that are assorted into multiple different independent claims in an unclear manner and result in a "maze of confusion." The Examiner contacted Applicants representative, Andrew Zidel, Reg No. 45,256, to allow Applicants the opportunity to provide a preliminary amendment to

> resolve the undue multiplicity. Applicants representative elected claims 1-12, 24-34, and 53-63 to be examined. **(See Section 2.iii above)**

(Office Action, p.7, numbered section 4, emphasis in original.)

Section 2.iii of the Office Action stated "[t]hese multiple combinations of limitations do not present a definition but rather a blur and a maze of confusion." This section went on to state **"The Examiner once again notes that Applicants did not disagree with the reasoning provided or the rejection itself when they elected claims 1-12, 24-34, and 53-63 to be examined."** (Emphasis in original.)

Appellant strongly disagrees with such assertions. In addressing rejections not based on prior art, the MPEP instructs that "[w]here a major technical rejection is proper (e.g., lack of proper disclosure, undue breadth, utility, etc.) **such rejection should be stated with a full development of the reasons rather than by a mere conclusion coupled with some stereotyped expression**." (MPEP § 706.03, emphasis added.) Unfortunately, the multiplicity rejection does exactly what the MPEP cautions against.

The phrases "a blur" and "a maze of confusion" merely parrot back catchphrases from caselaw without articulating an ascertainable reason for the rejection. *See, e.g., In re Flint*, 411, F.2d 1353, 1357, C.C.P.A. 1969 ("Such latitude, however, should not be extended to sanction that degree of repetition and multiplicity which beclouds definition in a maze of confusion") *quoting In re Chandler*, 319 F.2d 211 at 225, C.C.P.A. 1963). *See also In re Chandler*, 254 F.2d 396, C.C.P.A. 1958 ("it is proper to allow applicants a reasonable latitude in setting forth their inventive concepts in different phraseology, but it is the purpose of the claims to point out and define what an applicant regards as his invention, and that purpose is not served if, as the result of frequent repetitions, they present

to the mind a blur rather than a definition."). The catchphrases relied on in the Office Action do not satisfy the Examiner's initial burden when issuing a multiplicity rejection. In particular:

> **the examiner bears the initial burden**, on review of the prior art or **on any other ground, of presenting a *prima facie* case of unpatentability**. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant.

(*In re Oetiker*, 977 F.2d 1443, 1445, Fed. Cir. 1992, emphasis added.)

Appellant also refers to MPEP § 2107.02, which cites the above-quoted section of *In re Oetiker* and goes on to state that the "*prima facie* showing must be set forth in a well-reasoned statement." Appellant submits that a valid *prima facie* case for multiplicity was never made, necessitating the reversal of this rejection. While section 2.iii of the Office Action, which is quoted above, asserts that appellant did not disagree with the reasoning for the rejection, no such reasoning was provided and appellant has consistently traversed the rejection.

The original Office Action in this case referred to an Interview Summary which was attached to the Office Action. *See* May 3, 2007 Office Action, numbered section 4, p.4. The Interview Summary stated "[t]he Examiner contacted Applicants representative, Andrew Zidel, Reg No 45,256, to allow Applicants the opportunity to provide a preliminary amendment to resolve the undue multiplicity. Applicants representative elected claims 1-12, 24-34, and 53-63 to be examined." (Interview Summary, p.2.) As can be seen, no reasoning explaining the basis of the multiplicity rejection was set forth in the Interview Summary.

In response to the May 3, 2007 rejection, applicant replied as follows:

As an initial matter, applicant would like to thank the Examiner for the telephone discussion with the undersigned regarding the instant application. Applicant notes that the Examiner-Initiated Interview Summary contains a typographical error as to the date of the interview, which was conducted on April 26, 2007 rather than April 26, 2008. **Furthermore, to the best recollection of the undersigned, no preliminary amendment was discussed at that time. Rather, the Examiner provided applicant an opportunity to elect certain claims in view of an expected multiplicity rejection. In view of same and the Examiner's determination that three sets of claims would be examined, applicant provisionally elected claims 1-12, 24-34 and 53-63.**

The multiplicity rejection was made in the instant Office Action pursuant to 35 U.S.C. § 112, ¶ 2 in view of M.P.E.P. § 2173.05(n). **Applicant respectfully traverses the multiplicity rejection.**

The Office Action quotes a portion of § 2173.05(n) in support of the rejection. However, a critical portion of this section of the M.P.E.P. is omitted. Specifically, "Undue multiplicity rejections based on 35 U.S.C. 112, second paragraphs, should be applied judiciously and should be rare."

In support of the rejection, the Office Action states that the 89 claims, including 11 independent claims, "contain limitations from multiple embodiments that are assorted into multiple different independent claims in an unclear manner and result in a 'maze of confusion.'" (Office Action, numbered section 4, p.3.)

Applicant has paid $1,930 in extra claim fees for the 89 claims as filed. **The Office Action has not provided any concrete reason to justify the refusal to examine all the claims. This is contrary to case law, including case law cited by the M.P.E.P. concerning multiplicity. Specifically, it has been held that an Examiner should set forth "typical examples of substantial duplication or lack of material differentiation" among the claims, and that reliance on "mere opinion" is insufficient to support a multiplicity rejection.** *In re Flint*, 411 F.2d 1353, 1356, C.C.P.A. 1969. In *Flint*, the Court reversed a multiplicity rejection even though the examiner did set forth typical examples of substantial duplication.

> **Because the Office Action fails to set forth any concrete examples of undue multiplicity as asserted, it appears that reliance was made solely on the mere opinion of the Examiner. Applicant respectfully submits that for at least these reasons the rejection is improper and should be withdrawn.** In the alternative, applicant requests that the USPTO return the $1,930 paid in extra claim fees.

(June 21, 2007 Amendment, pp.19-20, emphasis added.)

Thus, appellant clearly showed that there was no proper reasoning behind the multiplicity rejection and expressly traversed the rejection. In response, the next Office Action stated that "the reasoning behind the rejection provided during the phone call, following Ex parte Joyce and Van Langenhoven, 169 USPQ 373 (Bd. Pat. App. & Int. 1969), was sufficient." (September 11, 2007 Office Action, p.3, numbered section 2.) However, as shown above, no grounds were articulated in the original Office Action or accompanying Interview Summary. Appellant's response to the September 11, 2007 Office Action reiterated that no grounds of rejection were set forth. Therefore, appellant again traversed the rejection and requested that it be withdrawn. Appellants' October 31, 2007 Amendment at pp.18-19 stated:

> Turning to the rejections as set forth in the September 11, 2007 final Office Action, applicant incorporates the arguments as set forth in the June 21, 2007 amendment as they apply as well to the final Office Action, with the exception being that the § 112, ¶ 2 rejection of claim 2 has been withdrawn.
>
> The multiplicity rejection was made in the instant Office Action pursuant to 35 U.S.C. § 112, ¶ 2 in view of M.P.E.P. § 2173.05(n). Applicant respectfully traverses the multiplicity rejection.
>
> In support of the rejection, the Office Action states that the 89 claims, including 11 independent claims, "contain limitations from multiple embodiments that are assorted into multiple different independent claims in an unclear manner and result in a 'maze of confusion.'" (Office Action, numbered section 4, p.7.)

> As explained previously, applicant has paid $1,930 in extra claim fees for the 89 claims as filed. The Office Action has not provided any concrete reason to justify the refusal to examine all the claims. This is contrary to case law, including case law cited by the M.P.E.P. concerning multiplicity. Specifically, it has been held that an Examiner should set forth "typical examples of substantial duplication or lack of material differentiation" among the claims, and that reliance on "mere opinion" is insufficient to support a multiplicity rejection. *In re Flint*, 411 F.2d 1353, 1356, C.C.P.A. 1969. In *Flint*, the Court reversed a multiplicity rejection even though the examiner did set forth typical examples of substantial duplication.
>
> Because the Office Action fails to set forth any concrete examples of undue multiplicity as asserted, it appears that reliance was made solely on the mere opinion of the Examiner. Applicant respectfully submits that for at least these reasons the rejection is improper and should be withdrawn. In the alternative, applicant requests that the USPTO return the $1,930 paid in extra claim fees.

Appellant submits that the Examiner has failed to provide the required *prima facie* case to establish the multiplicity rejection. No concrete examples of undue multiplicity, such as evidence of substantial duplication or lack of material differentiation, have ever been made of record in this case. The Examiner has failed to explain on the record which limitations (if any) of the pending claims are unclear. The Examiner has failed to state what is so confusing about the pending claims. Instead, the Office Actions in this case repeat conclusions coupled with regurgitated catchphrases from caselaw. This, without more, is sufficient to necessitate reversal of the rejection. Nonetheless, it will now be shown that the 11 independent claims and their associated dependent claims do not "result in a maze of confusion" as asserted in the appealed-from Office Action.

Of the claims on appeal, claims 1, 13, 24, 35, 44, 50, 53, 64, 65, 66 and 76 are independent. Claims 1, 13, 44, 50 and 66 are method claims. Claims 24, 35 and 76 are system claims. And claims 53, 64 and 65 are apparatus claims. Features and aspects of these claims will now be addressed.

Claim 1 is directed to a method of scheduling operations to be performed by a component having a thermal threshold. The method includes features such as determining a cooling attribute associating operations with a thermal attribute. Operations are scheduled in an order of performance based on the thermal and cooling attributes so that the thermal threshold is not exceeded.

Claim 13 is directed to thermal scheduling method that manipulates a series of operations by obtaining program code and determining thermal attributes associated with some of the operations. A thermal threshold for a component is determined and operations are scheduled so that the thermal threshold is not exceeded.

The method of claim 44 is directed to performing operations in a computing environment. A pair of operations is stored based on their thermal attributes, and one or both operations may be retrieved depending on a thermal threshold of a processor.

Claim 50 is direct to a method of performing operations, including determining if a processor's temperature exceeds a thermal threshold. Different operations may be executed depending upon which operations are available and whether the thermal threshold is exceeded.

And claim 66 presents a method of processing tasks. Here, a task may be selected based on an attribute which is

related to the temperature of a component after execution of a given task.

System claim 24 is directed to a processing system that includes a computing device with a component and a plurality of operations to be performed by the component. Some of the operations include a priority. At least one thermal attribute is associated with the component and a given operation. Claim 24 also provides a plurality of priority queues and a scheduler to assign operations to the component depending on the thermal attribute.

System claim 35 is directed to a processing system having a pair of operations each having a thermal attribute. One of the thermal attributes exceeds an operating threshold while the other does not. A scheduler manages the operations based on the thermal attributes, and processors may execute the operations.

And system claim 76 includes a memory for storing tasks to be processed as well as a component that processes the stored tasks. The tasks are associated with attributes which are related to the temperature of the component after a given task is processed.

Apparatus claim 53 is directed to a processing apparatus including a memory and a plurality of processing devices. The memory is for storing operations having thermal attributes, and includes a local store with a pair of queues. As recited, a first operation has a thermal attribute exceeding an operating threshold while a second operation has a thermal attribute which doe not exceed the operating threshold. At least one of the processors has a sub-processing unit and at least some of the processors have a thermal threshold and access to the memory. Different actions may occur depending on whether

the thermal threshold of a selected processing device is exceeded or not exceeded.

Apparatus claim 64 is directed to a processing apparatus for processing operations associated with thermal attributes. First and second memories store operations and a plurality of processing devices executes such operations. Depending on the thermal threshold of a selected processing device, different operations may be selected for processing.

And claim 65 is directed to an apparatus including a pair of memories and a number of processing devices. Operations may be obtained for processing depending on the thermal threshold of a given processing device.

As admitted by the Examiner and as explained by the MPEP, the "right of applicants to freedom of choice in selecting phraseology which truly points out and defines their inventions should not be infringed." (MPEP § 2173.05(n)) Furthermore:

> the mere fact that a larger number of claims are made than necessary to cover the invention is not sufficient to warrant rejection upon the ground of undue multiplicity of claims. In addition, to warrant a rejection on that ground, the claims must be not only of greater number than necessary to protect an invention, but they must be of a character "the net result of which is to confuse, rather than to clarify, the issues relative to an alleged improvement, which, it is claimed, involves the invention.

(*In re Savage*, 110 F.2d 680, 685, C.C.P.A. 1940; *see also In re Flint*, 411 F.2d 1353, C.C.P.A. 1969)

Appellant also refers to *In re Wakefield*, which held "an applicant should be allowed to determine the necessary number and scope of his claims, provided he pays the required fees and otherwise complies with the statute" (422 F.2d 897, 900, C.C.P.A. 1970.) *Wakefield* also noted that examination of dozens of claims in a single application "may be tedious work,

but this is no reason for saying that the invention is obscured by the large number of claims." (*Id.*)

In the present case, appellant has complied with the applicable statues and has paid the required fees, including additional claim fees amounting to nearly $2,000. Appellant submits that the claims on appeal, including the 11 independent claims, are clear and concise. There is no "maze of confusion." Furthermore, the appealed-from Office Action failed to provide any evidence which would support a *prima facie* case of multiplicity. Therefore, appellant respectfully submits that the rejection is improper and should be reversed.

II. The § 101 Statutory Subject Rejection of Claims 1-11, 24, 26-31, 33-34, 53-60 and 63

The Office Action states that the examined claims (1-11, 24, 26-31, 33-34, 53-60 and 63) are directed to non-statutory subject matter. Appellant respectfully disagrees.

A. Independent claim 1 and dependent claims 3-5, 8 and 10-11

The § 101 rejection of this independent claim was presented as follows: "Claim 1 recites providing, associating, and scheduling operations. Therefore the claim does not produce a useful, concrete, and tangible result. The resultant of the claims is neither stored, nor provided to a user, etc., for example, and therefore does not contain a concrete and tangible result. **(See Section 2.iv above)**" (February 4, 2008 Office Action, p.6, numbered section 3, emphasis in original.) Section 2.iv of the Office Action stated "The claims do not produce a tangible result. The generating an order of performance, scheduler, and obtaining an operation from memory do not represent tangible results. These limitations appear to be mere

data manipulation and as such are non-statutory." (*Id.* at p.3, numbered section 2.)

Per page 3 of the Office Action, the crux of the Examiner's position appears to be that no tangible result is produced. According to the MPEP:

> The tangible requirement does not necessarily mean that a claim must either be tied to a particular machine or apparatus or must operate to change articles or materials to a different state or thing. However, the tangible requirement does require that the claim must recite more than a 35 U.S.C. 101 judicial exception, in that the process claim must set forth a practical application of that judicial exception to produce a real-world result. *Benson*, 409 U.S. at 71-72, 175 USPQ at 676-77 (invention ineligible because had "no substantial practical application."). "[A]n application of a law of nature or mathematical formula to a … process may well be deserving of patent protection." *Diehr*, 450 U.S. at 187, 209 USPQ at 8 (emphasis added); see also *Corning*, 56 U.S. (15 How.) at 268, 14 L.Ed. 683 ("It is for the discovery or invention of some practical method or means of producing a beneficial result or effect, that a patent is granted . . ."). In other words, the opposite meaning of "tangible" is "abstract."

(MPEP § 2106(4)(C)(2)(b).)

Appellant submits that one practical application to produce a "real-world result" includes the claimed steps of "determining a cooling attribute; scheduling the operations in an order of performance based on the thermal attribute and the cooling attribute so that the thermal threshold is not exceeded; and generating the order of performance for use in execution of the operations." Without the order of performance obtained by the claimed process, the component could overheat and be damaged or degraded. This is explained in the specification as follows:

> Heat is often generated as components and devices perform operations such as instructions and tasks. Excessive heat can adversely impact the processing capability of an electronic component such as a

> computer chip. For example, if one area of the chip is performing computationally intensive tasks, that area can heat up significantly and form a hot spot relative to the rest of the chip. If the hot spot exceeds a thermal threshold, the performance of the components or devices in that area of the chip may be degraded, or the chip may even become damaged or destroyed.

(Specification paragraph 0004.)

Furthermore, the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63, stating: "paragraph 74 of the instant application recites, "The compiler may be implemented in software, firmware, hardware or a combination of the above." Therefore the claimed limitations may be entirely software and are therefore non-statutory since "software per se" does not fall under an approved statutory category. **(See Section 2.v above)**." (*Id.* at p.6, numbered section 3, emphasis in original.) Section 2.v of the Office Action stated:

> Applicants further argue the 101 rejections of the claims by stating that the claims do no positively recite a compiler. However as per the specification of the instant application the compiler is associated with the processing devices and components, see paragraph 76 of the instant application, and therefore since the claims recite these elements and a compiler is associated with these elements the 101 rejections are maintained. The claims are not being limited by the citation of the specification provided by the Examiner. **The Examiner is merely pointing out that the compiler can encompass software, and the claims need not explicitly recite the compiler since as per the specification the compiler is a clear part of the processing devices and components which are explicitly recited in the claims. The Examiner is puzzled by Applicants arguments since the compiler is a key part of Applicants invention, as can be seen in Figures 2 and 11**.

(*Id.* at p.3, numbered section 2, emphasis added.)

The assertion in section 2.v of the Office Action regarding the compiler is wholly without merit. The Examiner

did not set forth a rejection asserting that a compiler is an essential or critical feature which is unclaimed. While a compiler may be employed with the claimed invention, nothing in the specification requires such a structure to be part of claimed method. Thus, the Office Action's assertions about a compiler and "software per se" simply do not apply to this claim.

Additionally, it was pointed out to the Examiner in the October 31, 2007 amendment it is black letter law that it is improper to read limitations from the specification into the claims. (*See Teleflex, Inc. v. Ficosa N. Amer. Corp.*, 299 F.3d 1313 (Fed. Cir. 2002) ("limitations from the specification are not to be read into the claims.") (*Id.* at 1326)). Unfortunately, while clearly improper, this is exactly what the Examiner has done. In particular:

> as per the specification of the instant application **the compiler is associated with the processing devices and components**, see paragraph 76 of the instant application, **and therefore since the claims recite these elements and a compiler is associated with these elements the 101 rejections are maintained**.

(February 4, 2008 Office Action, p.3, numbered section 2, emphasis added.)

Paragraph 0076 of the specification recites:

> **In accordance with one aspect of the invention, a program compiler uses the thermal attributes to help prevent a component from overheating**. The compiler may be implemented in software, firmware, hardware or a combination of the above. It may be associated with (e.g., incorporated into) a processing element (such as PE 300 or PE 350) or subcomponent thereof. FIG. 11 illustrates compiler functionality in accordance with aspects of the invention. As is well known in the art, compilers receive source code and generate object code that can be run on a computing system. **According to aspects of the present invention, the compiler receives source code as well as thermal attributes relating to operations and/or components**. The compiler preferably generates object code based on the thermal

> attributes. As the compiler manages compilation by counting the number of instructions, the thermal attribute(s) of the object code compiled by the compiler is statically estimated. Enhanced thermal attribute determination is preferably made using a "profiler," which is a performance monitor that can count dynamic execution of the instructions and can report the operating frequency of each component. The profiler can provide more accurate thermal estimates to the compiler, which, in turn, will result in thermally optimized object code generation.

(Specification ¶ 0074, emphasis added.)

While one aspect of the invention may include a compiler, that is simply no reason to read this additional limitation into claim 1. Appellant is unaware of any law, rule, regulation or guideline finding that the mere "association" between two components necessitates reading in the omitted component into a claim. Thus, as claim 1 does not require a compiler, appellant submits that the discussion in the rejection regarding a compiler is erroneous and any rejection based on it should be reversed.

B. Dependent claim 2

Claim 2, which depends from claim 1, is statutory under § 101 not only because independent claim 1 contains statutory subject matter but also because the claim further requires the step of measuring the thermal attribute with a temperature sensing means. Examples of temperature sensing means are described in the specification, for instance at paragraphs 0070 ("a thermometer or other temperature sensing device") and 0087 ("thermal sensors"). Measurements using such tools result in a tangible result, namely the temperature of a given device or component.

Furthermore, as noted above with regard to claim 1 in section II(A), the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63. As

discussed above with regard to claim 1, the assertion in section 2.v of the Office Action regarding the compiler is wholly without merit. The Examiner did not set forth a rejection asserting that a compiler is an essential or critical feature which is unclaimed. While a compiler may be employed with the claimed invention, nothing in the specification requires such a structure to be part of claimed method. Thus, the Office Action's assertions about a compiler and "software per se" simply do not apply to this claim.

And as addressed above in section II(A) with regard to claim 1, it was pointed out to the Examiner in the October 31, 2007 amendment it is black letter law that it is improper to read limitations from the specification into the claims. (*See Teleflex, Inc. v. Ficosa N. Amer. Corp.*, 299 F.3d 1313 (Fed. Cir. 2002) ("limitations from the specification are not to be read into the claims.") (*Id.* at 1326)). The arguments and evidence presented above with regard to claim 1 apply to claim 2 and are hereby incorporated herein.

While one aspect of the invention may include a compiler, that is simply no reason to read this additional limitation into claim 2. Appellant is unaware of any law, rule, regulation or guideline finding that the mere "association" between two components necessitates reading in the omitted component into a claim. Thus, as claim 2 does not require a compiler, appellant submits that the discussion in the rejection regarding a compiler is erroneous and any rejection based on it should be reversed.

C. Dependent claim 6

Claim 6, which depends from claim 1, is statutory under § 101 not only because independent claim 1 contains statutory subject matter but also because the claim further

requires that the component execute the operations in the order of performance, which is clearly not an abstract activity.

Furthermore, as noted above with regard to claim 1 in section II(A), the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63. As discussed above with regard to claim 1, the assertion in section 2.v of the Office Action regarding the compiler is wholly without merit. The Examiner did not set forth a rejection asserting that a compiler is an essential or critical feature which is unclaimed. While a compiler may be employed with the claimed invention, nothing in the specification requires such a structure to be part of claimed method. Thus, the Office Action's assertions about a compiler and "software per se" simply do not apply to this claim.

And as addressed above in section II(A) with regard to claim 1, it was pointed out to the Examiner in the October 31, 2007 amendment it is black letter law that it is improper to read limitations from the specification into the claims. (*See Teleflex, Inc. v. Ficosa N. Amer. Corp.*, 299 F.3d 1313 (Fed. Cir. 2002) ("limitations from the specification are not to be read into the claims.") (*Id.* at 1326)). The arguments and evidence presented above with regard to claim 1 apply to claim 6 and are hereby incorporated herein.

While one aspect of the invention may include a compiler, that is simply no reason to read this additional limitation into claim 6. Appellant is unaware of any law, rule, regulation or guideline finding that the mere "association" between two components necessitates reading in the omitted component into a claim. Thus, as claim 6 does not require a compiler, appellant submits that the discussion in the rejection regarding a compiler is erroneous and any rejection based on it should be reversed.

D. Dependent claim 9

Claim 9, which depends from claims 1 and 8, is statutory under § 101 not only because independent claim 1 contains statutory subject matter but also because the claim further requires the steps of selecting processing devices, monitoring the devices and "routing the operations among the selected processing devices so that the individual thermal thresholds are not exceeded." Routing may be understood with reference to FIGS. 9A-C, which are explained in the specification as follows:

> FIG. 9A illustrates multiple PEs running a group of tasks. In this example, assume PE 2 overheats during its processing of task 1. **It is possible to move task 1 from PE 2 to one of the other processors, which may be operating other tasks, e.g., tasks 2 and 3**. The other tasks are preferably lower priority tasks then the one currently being performed by PE 2.
>
> As seen in FIG. 9B, **the task in the other processor, e.g., task 3, may be "swapped out" and sent to, e.g., the appropriate queue (or to a different processor).** Thus, PE 2 would not perform a task while PE 3 completes task 1. Alternatively, the two processors can swap tasks so that PE 2 performs the lower priority task as seen in FIG. 9C. As seen in FIG. 9C, (1) initially PE 2 and PE 3 may operate at standard clock speed of, e.g., 500 MHz. Then, (2) if PE 2 becomes hot while operating a high priority task 1, its task may be switched with lower priority task 3 of PE 3. **Finally, (3) the lower priority task 3 may be performed at a slower or reduced clock speed (e.g., 250 MHz), allowing PE 2 to cool off, while PE 3 continues execution of task 1 at the standard clock speed of 500 MHz**. It is also possible to increase the clock speed (e.g., to 650 MHz) to perform a higher priority task. It should be understood that the standard, increased and reduced clock speeds are merely exemplary, and may vary depending upon the specific architecture of the processor, sub-processor and/or maximum clock rate of the multiprocessing system. In a worst-case scenario, the overheating processor may halt operations until the temperature reaches a satisfactory level. However, the other processors in the multiprocessor system will continue

> processing so that real time operations and other critical operations are performed promptly. **While PEs are shown in FIGS. 9A-C, it is possible to perform the same operations with PUs and SPUs, or combinations of various processing devices. For example, an overheating SPU 308 may send its high priority task to the PU 304, which can reassign the task to a second SPU 308. Similarly, the PU 304 may take the lower priority task of the second SPU 308 and assign it to the first SPU 308. Once the first SPU 308 cools down, it may resume processing high priority and/or "hot" tasks at the normal clock speed.**

(Specification paragraphs 0095-0096, emphasis added.)

In view of the above, appellant respectfully submits that the claimed routing operation fully satisfies the requirements of § 101.

Furthermore, as noted above with regard to claim 1 in section II(A), the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63. As discussed above with regard to claim 1, the assertion in section 2.v of the Office Action regarding the compiler is wholly without merit. The Examiner did not set forth a rejection asserting that a compiler is an essential or critical feature which is unclaimed. While a compiler may be employed with the claimed invention, nothing in the specification requires such a structure to be part of claimed method. Thus, the Office Action's assertions about a compiler and "software per se" simply do not apply to this claim.

And as addressed above in section II(A) with regard to claim 1, it was pointed out to the Examiner in the October 31, 2007 amendment it is black letter law that it is improper to read limitations from the specification into the claims. (*See Teleflex, Inc. v. Ficosa N. Amer. Corp.*, 299 F.3d 1313 (Fed. Cir. 2002) ("limitations from the specification are not to be read into the claims.") (*Id.* at 1326)). The arguments and

evidence presented above with regard to claim 1 apply to claim 9 and are hereby incorporated herein.

While one aspect of the invention may include a compiler, that is simply no reason to read this additional limitation into claim 9. Appellant is unaware of any law, rule, regulation or guideline finding that the mere "association" between two components necessitates reading in the omitted component into a claim. Thus, as claim 9 does not require a compiler, appellant submits that the discussion in the rejection regarding a compiler is erroneous and any rejection based on it should be reversed.

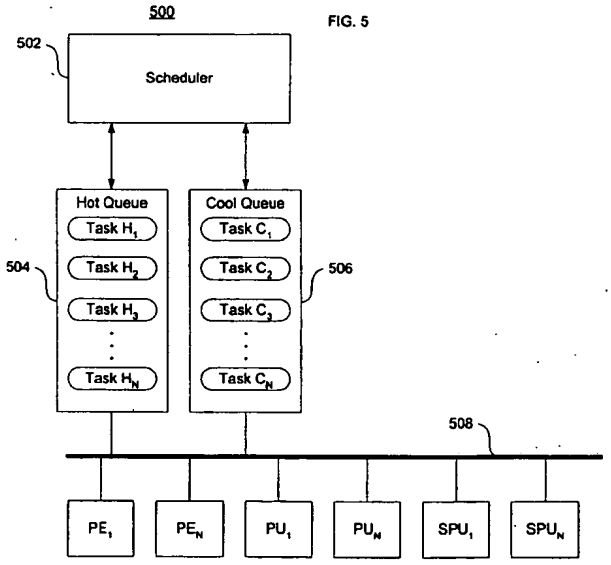
E. Independent claim 24 and dependent claims 26-31 and 33-34

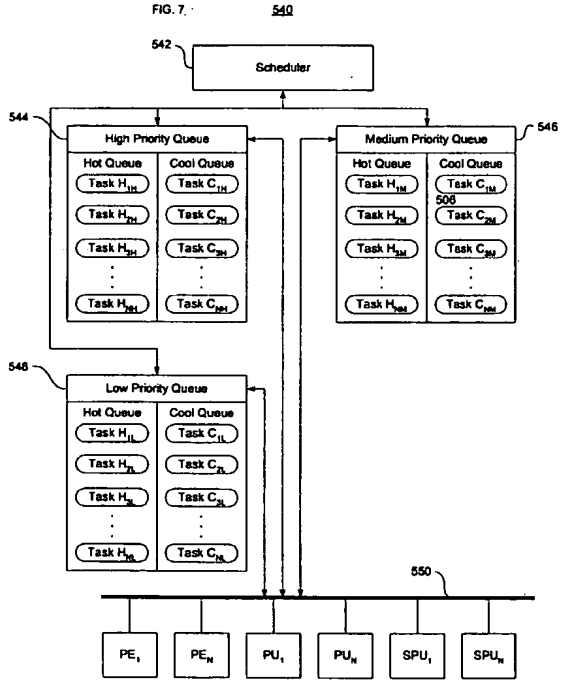
The § 101 rejection of independent claim 24 stated "Claim 24 recites a computing device with a plurality of associated operations. The association of operations appears to be mere data manipulation and therefore the claims do not produce a useful, concrete, and tangible result. **(See Section 2.iv above)**." (*Id.* at p.6, numbered section 3, emphasis in original.)

The above-quoted part of the § 101 rejection apparently focuses on a single clause in claim 24, namely "at least one thermal attribute associated with the component and a selected one of the operations." Unfortunately, the rejection ignores many other elements such as "a computing device including a component," "a plurality of operations to be performed by the component, at least some of the operations including a priority," " a plurality of priority queues," and "a scheduler." Appellant submits that when read in its entirety, claim 24 is directed to an apparatus that satisfies both the "transforms" and "produces a useful, concrete and tangible

result" prongs of the § 101 analysis as set forth in MPEPE § 2106.

By way of example only, in claim 24 each priority queue includes a first queue and a second queue. The first queue is for storing a first set of the operations and the second queue is for storing a second set of the operations. The scheduler is operable to assign at least one of the operations to the component depending on the thermal attribute. For instance, FIGS. 5 and 7 illustrate the use of multiple queues in conjunction with a scheduler. These figures are reproduced below.





In an embodiment of the invention discussed with regard to FIG. 5, the specification explains as follows:

> Reference is now made to FIG. 5, which illustrates a multi-queue scheduling methodology 500 in accordance with aspects of the present invention. **As seen in FIG. 5, a scheduler 502 is preferably associated with two queues.** For convenience, the first queue is referred

to herein as a "hot queue" 504 and the second queue is referred to herein as a "cool queue" 506. The queues 504, 506 may be implemented in many different ways, e.g., as data structures or a continuous or discontinuous collection in memory. In one example employing the SPUs 400, the queues 504, 506 are implemented external to the SPUs 400. The queues 504, 506 may also be implemented external to the PU 304 or the PE 300 (or PE 350), e.g., associated with the memory 330 (or memory 358). In another example, the queues 504, 506 are implemented internal to the SPUs 400. Desirably, the queues 504, 506 may be implemented in association with the local store 402 or the registers 404. For example, the hot queue 504 may be implemented in conjunction with the local store 402 of a first SPU 400 and the cool queue 506 may be implemented in conjunction with the local store 402 of a second SPU 400. In the case where an SPU 400 includes multiple local stores 402, the hot queue 504 may be stored in a first one of the local stores 402 while the cool queue 506 may be stored in a second one of the local stores 402 in the same SPU 400. Alternatively, both the hot queue 504 and the cool queue 506 may be implemented in the same local store 402 or in the same memory external to the SPU 400 or external to the PE 300. If the queues 504, 506 are implemented via the registers 404, various alternatives are possible. In one case, the hot queue 504 may be implemented via the register 404 of a first SPU 400 and the cool queue 506 may be implemented via the register 404 of a second SPU 400. The queues 504, 506 may also be implemented in a timesharing arrangement, for example where one of the queues 504, 506 is stored in a memory for a first period of time and then the other one of the queues 504, 506 is stored in the memory for a second period of time.

The scheduler 502 may populate the hot queue 504 and cool queue 506 with instructions, tasks or other operations, depending upon thermal attributes. Preferably, the scheduler 502 has access to a look-up table containing thermal attributes. The scheduler 502 may operate before and/or during runtime operation. **The scheduler 502 may choose a task from the hot queue 504 or the cool queue 506 depending upon the current (or predicted) temperature of a component. In a preferred example, so long as the current temperature of the device does not exceed an operating threshold, the scheduler 502 may select any task from either the**

hot or cool queues 504, 506. In another preferred example, if the operating threshold is not exceeded and if both hot and cool tasks are available, the scheduler 502 selects tasks from the hot queue 504 before selecting tasks from the cool queue 506. By way of example only, floating point instructions or tasks requiring multiple operations may be associated with a relatively high or positive thermal attribute value. These operations would be placed in the hot queue 504, e.g., as seen by tasks H_1 ... H_N. Other operations, such as integer instructions and single operation tasks, may be associated with a relatively low or negative thermal attribute. Such operations would be placed in the cool queue 506, e.g., as seen by tasks C_1 ... C_N. The thermal attribute of a task is preferably determined using information from the compiler and/or profiler, either of which may report the operating frequency of each component performing the task. More preferably, the thermal attribute of the task incorporates the operating frequency (e.g., the frequency of use) of the component(s), the thermal attribute of the component(s), and the cooling attribute. **In accordance with one embodiment, a simple scheduler only uses the total thermal attribute of a component that has sub-components, such as the SPU 400. In accordance with another embodiment, an advanced scheduler manages the thermal attributes of sub-components of the SPU such as the LS 402, the FPU 406 and the IU 408**. The table below illustrates thermal attributes for an IU, an FPU and an LS in a given SPU for a 3-D task and an MPEG-2 task.

(Specification paragraphs 0084-0085, emphasis added.)

Furthermore:

> as discussed above with regard to FIG. 5, if both hot and cool tasks are available and T_{max} is not exceeded, either a hot or a cool task may be selected. Thus, as seen by flow diagram 600, processing devices are able to avoid hot spots and overheating by selecting tasks from the hot and cool queues 504, 506. This process may be performed concurrently by one or more processing devices, thereby permitting execution of instructions and tasks without altering clock speed or shutting down the processing devices.

(Specification paragraph 0089.)

And in another embodiment of the invention discussed with regard to FIG. 7, the specification explains as follows:

> It is possible to combine the use of hot and cool queues with priority queues, as seen in FIG. 7. In this figure, a multi-queue scheduling methodology 540 is provided. **A scheduler 542 is associated with three priority queues, high priority queue 544, medium priority queue 546 and low priority queue 548, although different priority levels and numbers of queues may be employed. The scheduler 542 operates as described above with reference to the scheduler 502. Each of the priority queues 544, 546 and 548 preferably includes a hot queue and a cool queue, which are created and operate in the same manner described above with regard to FIG. 5.** For example, the high priority queue 544 has a hot queue for handling tasks H_{1H} ... H_{NH} and a cool queue for handling tasks C_{1H} ... C_{NH}. Similarly, the medium priority queue has a hot queue for handling tasks H_{1M} ... H_{NM} and a cool queue for handling tasks C_{1M} ... C_{NM}. The low priority queue has a hot queue for handling tasks H_{1L} ... H_{NL} and a cool queue for handling tasks C_{1L} ... C_{NL}.

(Specification paragraph 0090, emphasis added.)

Thus, the specification explains that because the queues can store different operations and the scheduler is operable to assign at least one operation to a component depending on, different operations may subsequently be acted on by the component in a manner that avoids hot spots and overheating. Operations are thus transformed by being placed in different queues for subsequent execution. And a concrete, useful and tangible result is the avoidance of hot spots and overheating when a component performs the operations. Therefore, appellant submits that independent claim 24 and dependent claims 26-31 and 33-34 satisfy the requirements of § 101.

Furthermore, as discussed above in section II(A) with regard to claim 1, the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63.

Appellant submits that the assertion in section 2.v of the Office Action regarding the compiler is wholly without merit.

The specification explains that a compiler is one type of scheduler. "FIGS. 2A-B illustrate how a compiler or other instruction scheduler can manage operations so as to avoid degradation of the processing or damage to the components." (Specification paragraph 0075.) The specification then explains that "the scheduler 502 may be implemented in hardware, firmware, or software. Preferably, the scheduler 502 is hardware-based and implemented in the PU 204. In another preferred alternative, the scheduler 502 is software-based as part of the operations system of the overall computing device." (Specification paragraph 0087.) While one embodiment of a scheduler may be software-based and implemented in a processing unit (PU), appellant submits that there is no support to the Examiner's contention that the claimed structure, including elements such as a computing device including a component, a plurality of priority queues and a scheduler, is "software per se." Appellant further submits that the Examiner has failed to establish the required *prima facie* case of unpatentability under § 101.

In view of the above, appellant requests that the § 101 rejection of independent claim 24 and associated dependent claims be vacated.

F. Independent claim 53 and dependent claims 54-60 and 63

Unlike the rejections of independent claims 1 and 24, the Examiner has not asserted that independent claim 53 does not produce "a useful, concrete and tangible result." Thus, as best understood, the sole basis for the § 101 rejection of

independent claim 53 and its dependent claims is due to an unclaimed feature, namely a compiler.

As discussed above in section II(A), the Office Action issued what appears to be a blanket § 101 rejection of claims 1-12, 24-34 and 53-63, stating: "paragraph 74 of the instant application recites, "The compiler may be implemented in software, firmware, hardware or a combination of the above." Therefore the claimed limitations may be entirely software and are therefore non-statutory since "software per se" does not fall under an approved statutory category. **(See Section 2.v above).**" (*Id.* at p.6, numbered section 3, emphasis in original.)

The assertion in section 2.v of the Office Action regarding the compiler is wholly without merit. The Examiner did not set forth a rejection of independent claim 53 asserting that a compiler is an essential or critical feature which is unclaimed. While a compiler may be employed with the claimed invention, nothing in the specification requires such a structure to be part of claimed method. Thus, the Office Action's assertions about a compiler and "software per se" simply do not apply to this claim.

It is black letter law that it is improper to read limitations from the specification into the claims. (*See Teleflex, Inc. v. Ficosa N. Amer. Corp.*, 299 F.3d 1313 (Fed. Cir. 2002) ("limitations from the specification are not to be read into the claims.") (*Id.* at 1326)). Unfortunately, while clearly improper, this is exactly what the Examiner has done, as discussed above in section II(A).

While one aspect of the invention may include a compiler, that is simply no reason to read this additional limitation into independent claim 53 or dependent claims 54-60 and 63. Appellant is unaware of any law, rule, regulation or

guideline finding that the mere "association" between two components necessitates reading in the omitted component into a claim. Thus, as independent claim 53 and dependent claims 54-60 and 63 do not require a compiler, appellant submits that the discussion in the rejection regarding a compiler is erroneous and any rejection based on it should be reversed.

III. The § 102 Rejection of Claims 1-11, 24, 26-31, 33-34, 53-60 and 63 as being anticipated by *Chauvel*

A. Claims 1-11

Claim 1 was previously amended to include the subject matter of dependent claim 12, which stands cancelled. Thus, claim 1 now includes "determining a cooling attribute" and "scheduling the operations in an order of performance based on the thermal attribute and the cooling attribute so that the thermal threshold is not exceeded."

The Office Action asserts that paragraph 0008 of *Chauvel* teaches the cooling attribute limitations of former claim 12. However, what paragraph 0008 of the reference actually states is:

> [0008] In addition to overall energy savings, in a complex processing environment, the ability to dissipate heat from the integrated circuit becomes a factor. An integrated circuit will be designed to dissipate a certain amount of heat. If tasks (application processes) require multiple systems on the integrated circuit to draw high levels of current, it is possible that the circuit will overheat, causing system failure or errant behavior.

As explained in the June 21, 2007 amendment, there is simply no teaching or suggestion in the cited portion of *Chauvel* or elsewhere of a cooling attribute as claimed. The "broadest reasonable interpretation" of the claimed cooling attribute should be understood in view of what the application describes.

See, for instance, specification paragraphs 0082-0087. The Office Action appears to ignore what a cooling attribute actually is as disclosed in the specification and instead points to the above-quoted paragraph in *Chauvel*. Applicant respectfully disagrees as this is wholly inconsistent with cooling attributes as disclosed in the instant application. For instance, specification paragraph 0082 recites:

> **[0082]** Preferably, a cooling attribute is associated with the computer chip containing the various components. The cooling attribute depends on the specific features of the cooling system of the computer chip. For example, the cooling attribute preferably depends on the chip packaging and cooler (such as a heat sink or a fan), if any. If the cooling system has only one state for the cooler (e.g., always operating the fan at a set rotation speed), the cooling attribute will be fixed. If the state of the cooling system can be altered, such as by changing the rotation speed of the fan, the cooling attribute is preferably dynamic, and may be determined or updated when the cooling system changes the operating state of the cooler. In one embodiment, the compiler uses a fixed cooling attribute calculated based upon a typical operational state of the cooler. The compiler uses the cooling attribute when calculating the density of operations belonging to specific components. More preferably, the compiler also factors in the heat dissipation capabilities of the chip packaging. In a further embodiment, the compiler or the profiler employs a dynamic cooling attribute to help the compiler perform object code generation. The table below illustrates an exemplary schedule for an integer operation that will be processed by a given integer unit (IU) 408 and a given local store (LS) 402 based upon thermal and cooling attributes.

And specification paragraph 0087 recites:

> **[0087]** As will be apparent to one skilled in the art, the scheduler 502 may be implemented in hardware, firmware, or software. Preferably, the scheduler 502 is hardware-based and implemented in the PU 204. In another preferred alternative, the scheduler 502 is

> software-based as part of the operations system of the overall computing device. The hot queue 504 and the cool queue 506 are preferably accessible to one or more PEs ($PE_1 \ldots PE_N$), PUs ($PU_1 \ldots PU_N$), and/or SPUs ($SPU_1 \ldots SPU_N$) during a program execution through a bus 508. In accordance with one embodiment, each PE, PU and/or SPU preferably includes thermal sensors (temperature sensing means) to monitor their temperature or, alternatively, estimate the current temperature. In accordance with another embodiment, each PE preferably includes a thermal sensor and an analog to digital A/D converter in order to provide a digital estimation of the temperature. Each kernel on the PE can preferably read its own digitized temperature at any time. The PEs, PUs and SPUs desirably each have a thermal threshold T_{max}, which can differ from component to component. If thermal sensors are not available, the current temperature may be calculated by the thermal attribute of the task and the current cooling attribute.

Appellant submits that the mere reference to heat dissipation as disclosed in paragraph 0008 of *Chauvel* does not teach or suggest the cooling attribute as claimed, even under the broadest reasonable interpretation permitted in view of the specification. Thus, for at least this reason, appellant submits that independent claim 1 is patentable over *Chauvel*. Furthermore, claims 2-11 depend from claim 1 and contain all the limitations thereof. In view of the above, appellant requests that the rejection of claim 1 and subject dependent claims 2-11 be reversed.

B. Claims 24, 26-30 and 33-34

With regard to independent claim 24, this claim recites, in part, "a plurality of operations to be performed by the component, at least some of the operations including a priority" and "a plurality of priority queues, each priority queue including a first queue and a second queue, the first queue for storing a first set of the operations and the second

queue for storing a second set of the operations." Thus, it can be seen that claim 24 refers to a dual queue configuration.

The February 4, 2008 Office Action referenced paragraph 0049 of *Chauvel*, without explanation, as purportedly teaching a plurality of priority queues. This section of *Chauvel* states:

> **[0049]** The power dissipation profile 102 can be computed from the events detected by various counters 78 associated with the components as shown in FIG. 9. A temperature field for the die may be computer from the dissipated power profile. When a critical power surge, such as the one shown at peak 114, is detected, a rescheduling of tasks may be computed by the power computing task 84. In this case, several solutions may be available to bring peak 114 down to an acceptable level. First, if the task running on MPU 12 was a high priority task, it might be possible to reschedule lower priority tasks on DSP1 14a or DSP2 14b. Since the power dissipation in the areas designated by DSP1 14a and DSP2 14b contribute to the power dissipation in the area designated by MPU 12, rescheduling one or more of the tasks using DSP1 14a or DSP2 14b may reduce the peak. Alternatively, it may be possible to reduce the power dissipation shown at peak 114 by reducing the frequency of the MPU 12, DSP1 14a and DSP2 14b.

While this relied-on section of *Chauvel* discloses the possibility of rescheduling lower priority tasks on either DSP1 or DSP2, appellant submits that it does not teach or otherwise suggest the dual priority queue structure of claim 24.

For the sake of completeness, appellant notes that in rejecting now cancelled claims 32 and 62, the May 3, 2007 Office Action asserted that *Chauvel* disclosed a plurality of priority queues by citing to a different section of the reference. Specifically, that Office Action asserted that paragraph 0030 of *Chauvel* disclosed a dual queue configuration. However, what this paragraph of *Chauvel* actually states is:

> **[0030]** Referring to **FIGS. 1 and 2**, the operation of the multiprocessor system **10** is discussed. The multiprocessor system **10** can execute a variety of tasks. A typical application for the multiprocessor system **10** would be in a smartphone application where the multiprocessor system **10** handles wireless communication, video and audio decompression, and user interface (i.e., LCD update, keyboard decode). In this application, the different embedded systems in the multiprocessor system **10** would be executing multiple tasks of different priorities. Typically, the OS would perform the task scheduling of different tasks to the various embedded systems.

Appellant further submits that nothing in this cited section or elsewhere in *Chauvel* teaches or suggests the first and second queues as claimed. Appellant respectfully submits that a queue is not "merely a schedule of tasks" as asserted in the rejection.

Thus, for at least these reasons, appellant submits that independent claim 24 is patentable over *Chauvel*. Furthermore, claims 26-31 and 33-34 depend from claim 24 and contain all the limitations thereof. In view of the above, appellant requests that the rejection of claim 24 and the subject dependent claims be vacated.

C. Claim 31

This claim depends from claim 30, which in turn depends from claim 24. Claim 31 requires that "the task thermal attribute is based on at least one of an operating frequency of the component, a thermal attribute of the component, and a cooling attribute." In the rejection of claim 31, the Office Action merely references paragraph 0008 and 0039 of *Chauvel* as purportedly disclosing these limitations.

Chauvel's paragraph 0008 was quoted above in section III(A). Paragraph 0039 is reproduced below.

[0039] where, f is the frequency, V_{dd} is the supply voltage and α is the probabilistic (or measured, see discussion in connection with block 76 of this figure) activity. In other words, $\sum_T(\alpha)*Cpd*f*V_{dd}$ is the energy corresponding to a particular hardware module characterized by equivalent dissipation capacitance Cpd; counters values give $\sum_T(\alpha)$ and E is the sum of all energies for all modules in the multiprocessor system 10 dissipated within T. Average system power dissipation W=E/T. In the preferred embodiment, measured and probabilistic energy consumption is calculated and the average power dissipation is derived from the energy consumption over period T. In most cases, energy consumption information will be more readily available. However, it would also be possible to calculate the power dissipation from measured and probabilistic power consumption.

Appellant submits that the mere reference to heat dissipation as disclosed in paragraph 0008 and the energy calculations and power dissipation discussion in paragraph 0039 of *Chauvel* do not teach or suggest that a task thermal attribute is based on an operating frequency of a component, a thermal attribute of a component, or a cooling attribute as claimed. Thus, for at least these reasons, appellant submits that claim 31 is patentable over *Chauvel*.

D. Claims 53-60

With regard to independent claim 53, this claim recites, in part, "wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device is operable to obtain the first operation from the memory for processing and to process the first operation, and if the thermal threshold of the selected processing device is exceeded, the selected processing device is operable to obtain the second operation from the memory for processing and to process the second operation, and wherein the memory

comprises a local store in the sub-processing unit, and the local store includes a first queue for managing the first operation and a second queue for managing the second operation."

Claim 53 thus refers to a dual queue configuration for managing different operations. Similar to the rejection of claim 24, the rejection of claim 53 merely referenced paragraph 0049 of *Chauvel*, without explanation, as purportedly teaching a dual priority queue structure. Paragraph 0049 of *Chauvel* is quoted above in section III(B). Appellant submits, as explained above with regard to claim 24, that while *Chauvel* discloses the possibility of rescheduling lower priority tasks on either DSP1 or DSP2, it does not teach or otherwise suggest the dual priority queue structure as presently claimed.

As discussed above in section III(B), in rejecting now cancelled claims 32 and 62, the May 3, 2007 Office Action asserted that *Chauvel* disclosed a plurality of priority queues by citing to a different section of the reference. Specifically, that Office Action asserted that paragraph 0030 of *Chauvel* disclosed a dual queue configuration. This paragraph of *Chauvel* is quoted above in section III(B). Appellant further submits that nothing in paragraph 0030 or elsewhere in *Chauvel* teaches or suggests the first and second queues as claimed. Appellant respectfully submits that a queue is not "merely a schedule of tasks" as asserted in the rejection.

Thus, for at least these reasons, appellant submits that independent claim 53 is patentable over *Chauvel*. Furthermore, claims 54-60 depend from claim 53 and contain all the limitations thereof. In view of the above, appellant requests that the rejection of claim 53 and the subject dependent claims be vacated.

E. Claim 63

This claim depends from independent claim 53 and recites "wherein the first and second operations are maintained in the memory in a timesharing arrangement." An example of this may be found with regard to the structure illustrated in FIG. 5, where two queues 504 and 506 are shown. As stated in paragraph 0084 of the specification, the "queues 504, 506 may also be implemented in a timesharing arrangement, for example where one of the queues 504, 506 is stored in a memory for a first period of time and then the other one of the queues 504, 506 is stored in the memory for a second period of time." (Specification paragraph 0084, p.26, l.34 to p.27, l.4.)

The Office Action merely references paragraph 0030 of *Chauvel* as anticipating claim 63. This paragraph, which is reproduced above in section III(B), discloses that a multiprocessor system can execute a variety of tasks, including tasks of different priorities. According to the paragraph, "Typically, the OS would perform the task scheduling of different tasks to the various embedded systems."

However, appellant submits that nothing in the relied-on section of *Chauvel* either discloses or suggests the features as set forth in claim 63, in particular the timesharing arrangement of the operations maintained in memory. Thus, appellant respectfully requests that the anticipation rejection based on *Chauvel* be withdrawn.

In view of the above, a reversal of the rejections of claims 1-11, 13-24, 26-31, 33-60 and 63-89 is respectfully requested.

Dated: June 26, 2008

Respectfully submitted,

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CLAIMS APPENDIX

1. (rejected) A method of scheduling operations to be performed by a component having a thermal threshold comprising:

providing a plurality of operations to be performed by the component;

associating the operations with a thermal attribute, the thermal attribute representing a value related to a heat amount expected to be generated or incurred by the component during performance of the operations;

determining a cooling attribute;

scheduling the operations in an order of performance based on the thermal attribute and the cooling attribute so that the thermal threshold is not exceeded; and

generating the order of performance for use in execution of the operations.

2. (rejected) The method of claim 1, further comprising measuring the thermal attribute with a temperature sensing means.

3. (rejected) The method of claim 1, further comprising estimating the thermal attribute based upon power consumption of the component.

4. (rejected) The method of claim 3, wherein estimating the thermal attribute further includes performing a circuit simulation of the component.

5. (rejected) The method of claim 3, wherein estimating the thermal attribute further includes determining a power density of the component.

6. (rejected) The method of claim 1, further comprising the component executing the operations in the order of performance.

7. (rejected) The method of claim 6, wherein the component includes a plurality of processing devices and the thermal attribute is an aggregate thermal attribute of selected ones of the processing devices that execute the operations.

8. (rejected) The method of claim 1, wherein the component includes a plurality of processing devices, each of the processing devices has an individual thermal threshold, and the thermal attribute includes a plurality of individual thermal attributes, each individual thermal attribute being associated with one of the processing devices.

9. (rejected) The method of claim 8, further comprising:

selecting at least some of the processing devices to execute the operations;

monitoring the selected processing devices; and

routing the operations among the selected processing devices so that the individual thermal thresholds are not exceeded.

10. (rejected) The method of claim 1, wherein the component includes a plurality of processing devices and the thermal attribute is allocated among the plurality of processing devices.

11. (rejected) The method of claim 1, further comprising determining the thermal attribute by:

(i) determining power consumption of the component;

(ii) determining a footprint of the component;

(iii) dividing the power consumption of the component by the footprint of the component to obtain per-area power consumption; and

(iv) multiplying the per-area power consumption by a thermal estimation constant.

12. (cancelled)

13. (rejected) A thermal scheduling method, comprising:

obtaining program code including a series of operations;

determining thermal attributes associated with one or more of the operations;

determining a thermal threshold for a component; and

scheduling the operations for execution by the component in accordance with the thermal attributes so that the thermal threshold is not exceeded.

14. (rejected) The method of claim 13, wherein the thermal attributes account for an amount of heat expected to be generated as the component executes a selected operation.

15. (rejected) The method of claim 13, wherein the thermal attributes account for an amount of heat generated over a period of time.

16. (rejected) The method of claim 13, wherein the thermal attributes account for at least one of power consumption of the component and power density of the component.

17. (rejected) The method of claim 13, further comprising:

the component executing the operations;

monitoring the temperature of the component during execution; and

rescheduling the operations if the thermal threshold is exceeded.

18. (rejected) The method of claim 13, further comprising estimating the thermal attributes by counting the number of tasks to be performed in each of the operations.

19. (rejected) The method of claim 13, wherein the component includes a plurality of processing devices, the method further comprising:

monitoring a dynamic execution of selected ones of the operations by selected ones of the processing devices;

determining an operational frequency of the selected processing devices; and

reporting the operational frequency of the selected processing devices to a compiler.

20. (rejected) The method of claim 13, further comprising:

determining a cooling attribute for a computing device, the computing device including the component;

wherein scheduling the operations is performed in accordance with the cooling attribute and the thermal attribute.

21. (rejected) The method of claim 20, wherein the cooling attribute is based on a type of packaging of the computing device.

22. (rejected) The method of claim 21, wherein the cooling attribute is further based on a cooling means of the computing device.

23. (rejected) The method of claim 22, wherein:

if the cooling means has one state, the cooling attribute is fixed; and

if the cooling means has multiple states, the cooling attribute is dynamic.

24. (rejected) A processing system comprising:

a computing device including a component;

a plurality of operations to be performed by the component, at least some of the operations including a priority;

at least one thermal attribute associated with the component and a selected one of the operations, the thermal attribute being indicative of a change in temperature of the component after performance of the selected operation;

a plurality of priority queues, each priority queue including a first queue and a second queue, the first queue for storing a first set of the operations and the second queue for storing a second set of the operations; and

a scheduler operable to assign at least one of the operations to the component depending on the thermal attribute.

25. (cancelled)

26. (rejected) The processing system of claim 24, wherein the scheduler is operable to retrieve a chosen one of the operations from a storage location depending upon the thermal attribute.

27. (rejected) The processing system of claim 24, wherein the component includes a plurality of sub-components, the scheduler is a simple scheduler, and the thermal attribute is a total thermal attribute associated with the component and not associated with the plurality of sub-components.

28. (rejected) The processing system of claim 24, wherein the component includes a plurality of sub-components, the scheduler is an advanced scheduler, and the thermal attribute is further associated with at least some of the sub-components.

29. (rejected) The processing system of claim 24, wherein the component is a processing device and the scheduler is integrated with the processing device.

30. (rejected) The processing system of claim 24, wherein the selected operation comprises a task, and the thermal attribute is a task thermal attribute.

31. (rejected) The processing system of claim 30, wherein the task thermal attribute is based on at least one of an operating frequency of the component, a thermal attribute of the component, and a cooling attribute.

32. (cancelled)

33. (rejected) The processing system of claim 24, further comprising a scheduler operable to assign at least some of the operations to either the first or the second queue in a selected one of the priority queues based on the priorities of the operations and on the thermal attribute.

34. (rejected) The processing system of claim 33, wherein the scheduler is further operable to retrieve a chosen one of the operations from the first queue or the second queue of the selected priority queue depending upon the thermal attribute and the priority of the chosen operation.

35. (rejected) A processing system, comprising:

a first operation having a first thermal attribute exceeding an operating threshold;

a second operation having a second thermal attribute not exceeding the operating threshold;

a scheduler for managing a plurality of operations comprising the first and second operations based on the thermal attributes; and

a plurality of processors for executing the plurality of operations, each of the plurality of processors having a thermal threshold.

36. (rejected) The processing system of claim 35, wherein if the thermal threshold of a selected one of the plurality of processors is not exceeded, the selected processor is operable to obtain and execute at least one of the first operation and the second operation.

37. (rejected) The processing system of claim 36, wherein, if the thermal threshold of the selected processor is not exceeded, the selected processor obtains the first operation.

38. (rejected) The processing system of claim 35, wherein, if the thermal threshold of a selected one of the plurality of processors is exceeded, the selected processor is operable to obtain and execute the second operation.

39. (rejected) The processing system of claim 35, wherein the processors include temperature sensing means for monitoring or estimating temperatures of the processors.

40. (rejected) The processing system of claim 39, wherein each processor further includes an analog to digital converter that is operable to receive a temperature value from the temperature sensing means and to provide a digital temperature value.

41. (rejected) The processing system of claim 35, wherein a selected one of the processors includes a plurality of sub-processors.

42. (rejected) The processing system of claim 41, wherein the selected processor has a total thermal attribute associated with the selected processor and not associated with the sub-processors.

43. (rejected) The processing system of claim 41, wherein each sub-processor has a component thermal attribute distinct

from the component thermal attributes of the other sub-processors.

44. (rejected) A method of performing operations in a computing environment, comprising:

storing a first operation based upon a thermal attribute of the first operation;

storing a second operation based upon a thermal attribute of the second operation; and

retrieving at least one of the first and the second operations depending upon a thermal threshold of a processor.

45. (rejected) The method of claim 44, wherein, if the thermal threshold of the processor is not exceeded, at least one of the first operation and the second operation is retrieved.

46. (rejected) The method of claim 45, wherein only the first operation is retrieved.

47. (rejected) The method of claim 44, wherein if the thermal threshold of the processor is exceeded, the second operation is retrieved.

48. (rejected) The method of claim 44, further comprising:

determining a priority of the first operation;

determining a priority of the second operation; and

providing a plurality of priority queues, each of the priority queues including a first queue and a second queue;

wherein the first operation is stored in one of the first queues based upon the priority of the first operation, and the second operation is stored in one of the second queues based upon the priority of the second operation.

49. (rejected) The method of claim 44, further comprising:

associating a component thermal attribute with the processor;

wherein retrieving the at least one operation further includes evaluating a current state of the component thermal attribute and selecting the at least one operation based upon the component thermal attribute.

50. (rejected) A method of performing operations in a computing environment, comprising:

determining if a temperature of a processor exceeds a thermal threshold; and

(i) if the thermal threshold is not exceeded:

determining if a first operation is available, the first operation being likely to maintain or increase the temperature of the processor upon execution; and

if the first operation is available, executing the first operation;

(ii) if the thermal threshold is exceeded:

determining if a second operation is available, the second operation being likely to decrease the temperature of the processor upon execution; and

if the second operation is available, executing the second operation.

51. (rejected) The method of claim 50, further comprising performing a nop if the second operation is not available.

52. (rejected) The method of claim 50, further comprising:

determining a priority level;

determining if the first operation is available from a priority queue of the priority level; and

if the first operation is not available from the priority queue, determining if the second operation is available from the priority queue.

53. (rejected) A processing apparatus for processing operations associated with thermal attributes, comprising:

a memory for storing a first operation and a second operation, the first operation having a thermal attribute exceeding an operating threshold, and the second operation having a thermal attribute not exceeding the operating threshold; and

a plurality of processing devices for executing the first and second operations, at least a selected one of the processing devices comprising a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the memory;

wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device is operable to obtain the first operation from the memory for processing and to process the first operation, and

if the thermal threshold of the selected processing device is exceeded, the selected processing device is operable to obtain the second operation from the memory for processing and to process the second operation, and

wherein the memory comprises a local store in the sub-processing unit, and the local store includes a first queue for managing the first operation and a second queue for managing the second operation.

54. (rejected) The processing apparatus of claim 53, wherein at least some of the processing devices are processing elements.

55. (rejected) The processing apparatus of claim 54, wherein at least some of the processing elements further comprise at least one sub-processing unit.

56. (rejected) The processing apparatus of claim 55, wherein each sub-processing unit includes a floating point unit, an integer unit and a register associated with the floating point unit and the integer unit.

57. (rejected) The processing apparatus of claim 56, wherein each sub-processing unit further includes a local store.

58. (rejected) The processing apparatus of claim 54, wherein at least some of the processing elements further comprise a processing unit and a plurality of sub-processing units associated with the processing unit.

59. (rejected) The processing apparatus of claim 58, wherein the sub-processing units each further include a local store.

60. (rejected) The processing apparatus of claim 53, wherein a first one of the processing devices is operable to exchange operations with a second one of the processing devices depending upon the thermal threshold of the first processing device.

61-62. (cancelled)

63. (rejected) The processing device of claim 53, wherein the first and second operations are maintained in the memory in a timesharing arrangement.

64. (rejected) A processing apparatus for processing operations associated with thermal attributes, comprising:

first and second memories for storing first and second operations, the first operation having a thermal attribute exceeding an operating threshold, and the second operation having a thermal attribute not exceeding the operating threshold;

a plurality of processing devices for executing the first and second operations, at least a selected one of the processing devices comprising a processing element, a processing unit or a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the first and second memories;

wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing device obtains the first operation from either the first memory or the second memory for processing, and

if the thermal threshold of the selected processing device is exceeded, the selected processing device obtains the second operation from either the first memory or the second memory for processing.

65. (rejected) A processing apparatus for processing operations associated with thermal attributes, comprising:

first and second memories for storing first and second sets of the operations, the first memory including a first queue for managing the first set of operations, the second memory including a second queue for managing the second set of operations, the first set of operations having thermal attributes exceeding an operating threshold, and the second set of operations having thermal attributes not exceeding the operating threshold;

a plurality of processing devices for executing the first and second sets of operations, at least a selected one of the processing devices comprising a processing element, a processing unit or a sub-processing unit, and at least some of the processing devices having a thermal threshold and access to the first and second memories;

wherein, if the thermal threshold of the selected processing device is not exceeded, the selected processing

device obtains at least one of the first set of operations for processing, and

if the thermal threshold of the selected processing device is exceeded, the selected processing device obtains at least one of the second set of operations for processing.

66. (rejected) A method of processing tasks comprising:

selecting one of a plurality of tasks for execution by a component based on an attribute, wherein the attribute for each task is related to the temperature of the component after execution of the associated task; and

executing the selected task.

67. (rejected) The method of claim 66 wherein the attribute is related to an expected increase or decrease in temperature of the component after execution of the associated task.

68. (rejected) The method of claim 67 wherein the expected increase or decrease is based on the power density of the component.

69. (rejected) The method of claim 66 wherein the tasks are stored in at least one queue in memory.

70. (rejected) The method of claim 66 wherein the tasks are stored in at least two queues in memory, one queue storing tasks whose attributes meet a condition and another queue storing tasks whose attributes do not meet the condition.

71. (rejected) The method of claim 66 wherein the condition is that the attribute exceeds a threshold.

72. (rejected) The method of claim 66 wherein the task is also selected based on the current temperature of the component.

73. (rejected) The method of claim 66 wherein the tasks are stored in different addresses in memory prior to execution.

74. (rejected) The method of claim 66 wherein the tasks are stored in the same address at different times in memory prior to execution.

75. (rejected) The method of claim 66 wherein the component is a processor.

76. (rejected) A system for processing tasks comprising:

memory for storing tasks to be processed;

a component that processes the tasks stored in the memory;

wherein the tasks are associated with attributes, the attribute for each task is related to the temperature of the component after processing the associated task, and one of the tasks is chosen for processing by the component based on the attribute.

77. (rejected) system of claim 76 wherein the attribute is related to an expected increase or decrease in temperature of the component after processing of the chosen task.

78. (rejected) The system of claim 77 wherein the expected increase or decrease is based on the power density of the component.

79. (rejected) The system of claim 76 wherein the tasks are stored in at least one queue in memory.

80. (rejected) The system of claim 76 wherein the tasks are stored in at least two queues in memory, one queue storing tasks whose attributes meet a condition and another queue storing tasks whose attributes do not meet the condition.

81. (rejected) The system of claim 80 wherein the condition is that the attribute exceeds a threshold.

82. (rejected) The system of claim 76 wherein the memory comprises two separate collections of memory, one collection of memory storing tasks whose attributes meet a condition and another collection of memory storing tasks whose attributes do not meet the condition.

83. (rejected) The system of claim 82 wherein the two separate collections of memory are stored at the same memory address but at different time periods.

84. (rejected) The system of claim 82 wherein the two separate collections of memory are at different memory addresses.

85. (rejected) The system of claim 84 wherein the two separate collections of memory are in the same semiconductive device.

86. (rejected) The system of claim 82 wherein the two separate collections of memory are in different semiconductive devices.

87. (rejected) The system of claim 76 wherein the component includes a temperature sensor and the task is selected based on an output of the temperature sensor.

88. (rejected) The system of claim 76 further comprising a second component capable of processing the tasks, wherein one or more of the tasks are selected for each component based on an expected temperature of each component after processing the task.

89. (rejected) The system of claim 76 further comprising a scheduler that selects one or more of the tasks for the component.

EVIDENCE APPENDIX

No evidence has been submitted pursuant to 37 C.F.R. §§ 1.130, 1.131 or 1.132 which is relied upon by appellant in the appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings as discussed in the section entitled "Related Appeals and Interferences."

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